Digital Electronics.

CHAPTER TWENTY THREE

CMOS Inverter

Introduction

Complementary MOS (CMOS) uses a P-channel MOS as a pull-up load device with an N-channel MOS as a pull-down device.

CMOS is widely used in digital circuit technology because it possesses the lowest power dissipation (wrist watches, hand-held calculators, and recently note book computers) and has the highest packing density.

All modern microprocessors are manufactured using CMOS technology including Intel's 80286, 80386, 80486, 8086, 8088 and Motorola's 68010,68020,68030, 68040

In this chapter, we will describe the operation of CMOS as an inverter device, and then analyze its VTC, power-dissipation, and fan-out.

Operation of CMOS Inverter

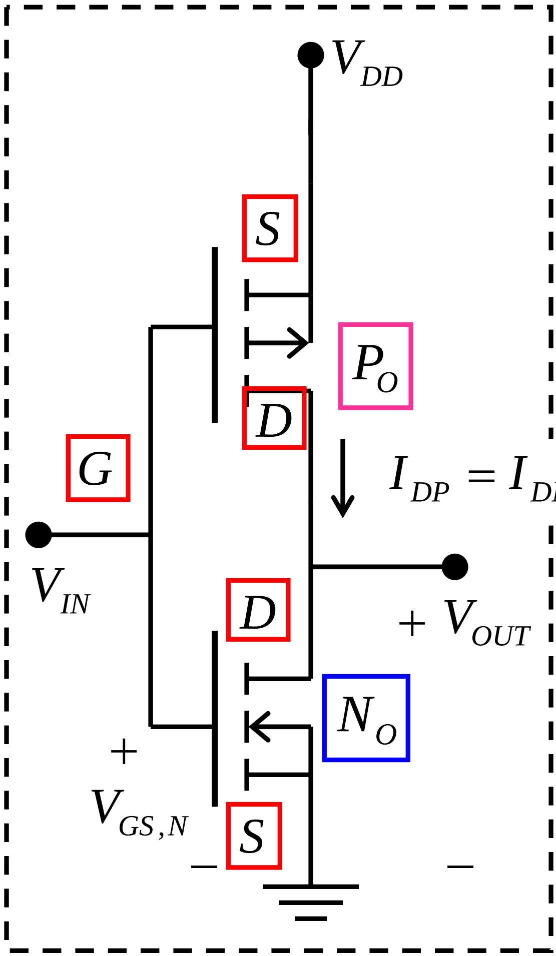
The drain terminal of the NMOS is connected with the drain terminal of the PMOS

$$\boxed{V_{IN} = V_{GS,N} = V_{DD} - V_{SG,P}}$$

The output is taken at the common drain terminal

$$\boxed{V_{OUT} = V_{DS,N} = V_{DD} - V_{SD,P}}$$

Note: either MOS can be considered as a load for the other, therefore the operations of N_O and P_O complement each other.



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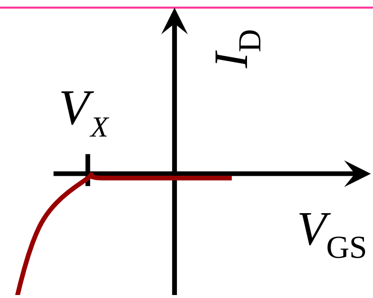
VTC of CMOS Inverter

$\boxed{V_{OH}}$

When $V_{IN}=0$, i.e. $V_{IN}=V_{GS,N}<V_{TN}$: → N_O is cut-off

$$I_{D,N}=I_{D,P}=0$$

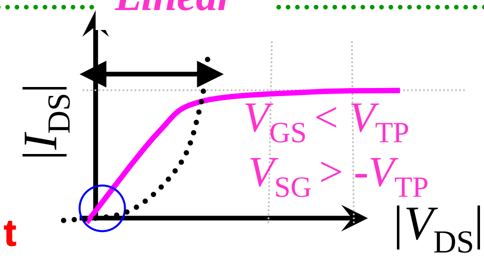


<u>P_O</u> $V_{SG,P}=V_{DD}-V_{IN}=V_{DD}$

$$V_{GS,P}=-V_{DD}<V_{TP}$$

→ Channel is created between the source and the drain of P_O MOS

Linear



In active mode: $(V_{GS} \le V_{TP})$

Zero drain current

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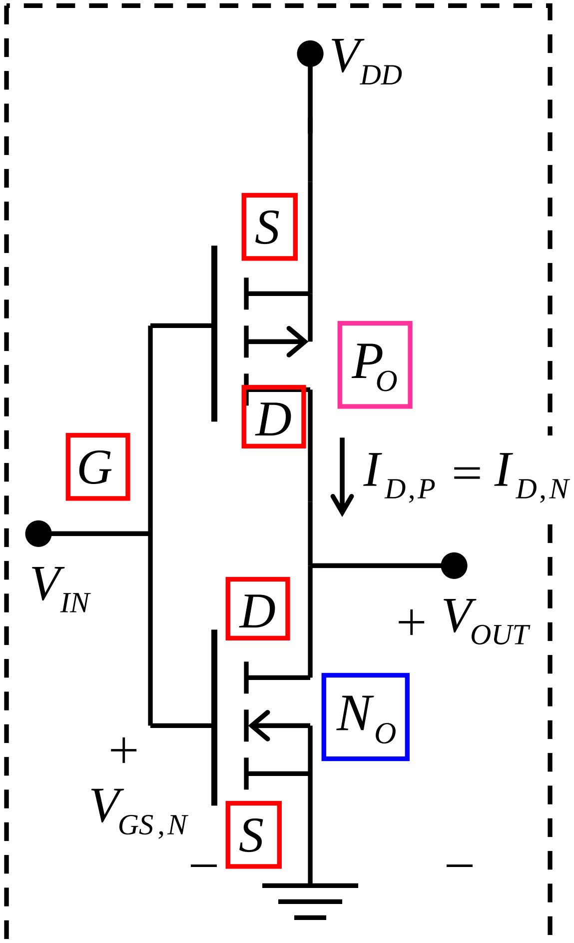
→ P_O is active (linear) mode



VTC of CMOS Inverter

$\boxed{V_{OH}}$

When $V_{IN}=0$, i.e. $V_{IN}=V_{GS,N}<V_{TN}$: → N_O is cut-off

$$I_{D,N} = I_{D,P} = 0$$

→ P_O is active (linear) mode

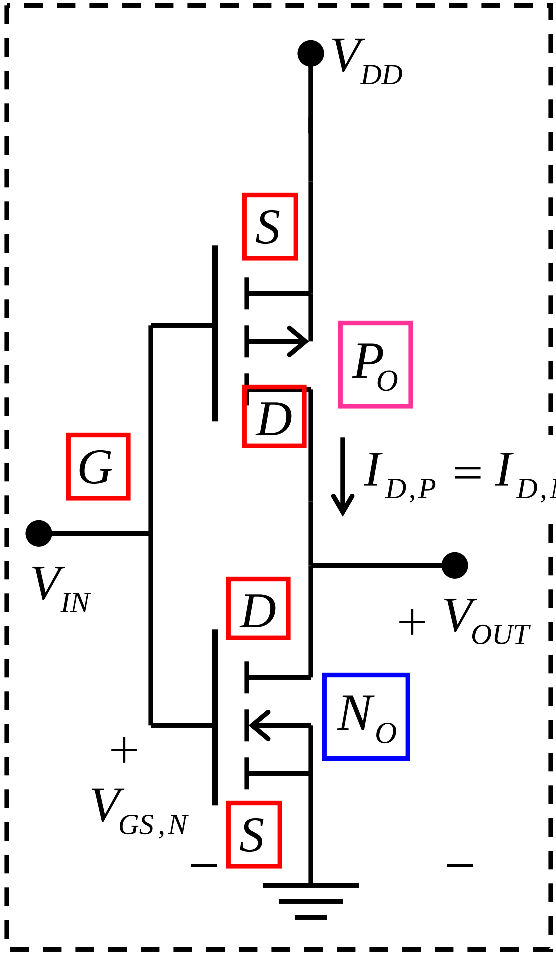
$$\boxed{I_{SD,P}(LIN) = \frac{K_p}{2}\left[2\times(V_{SG,P}+V_{TP})V_{SD,P} - V_{SD,P}^2\right] = 0}$$

$$V_{SD,P}\left\{2\times(V_{SG,P}+V_{TP}) - V_{SD,P}\right\} = 0$$

$$V_{SD,P} = 0$$

$$V_{SD,P} = 2\times(V_{SG,P}+V_{TP}) > V_{SG,P}+V_{TP}$$

$$\boxed{V_{OH} = V_{DS,N} = V_{DD} - V_{SD,P} = V_{DD}}$$



Invalid since V_{SD} has to be less than $(V_{SG}+V_{TP})$

VTC of CMOS Inverter

$\boxed{V_{OL}}$

For $V_{IN}=V_{OH}=V_{DD}$. $(V_{SG,P}=0 > V^{(-)}_{T,P})$

→ P_O is cut-off

Active mode: $(V_{GS} \geq V_{TN})$ **Zero drain current**

→ N_O is active, linear

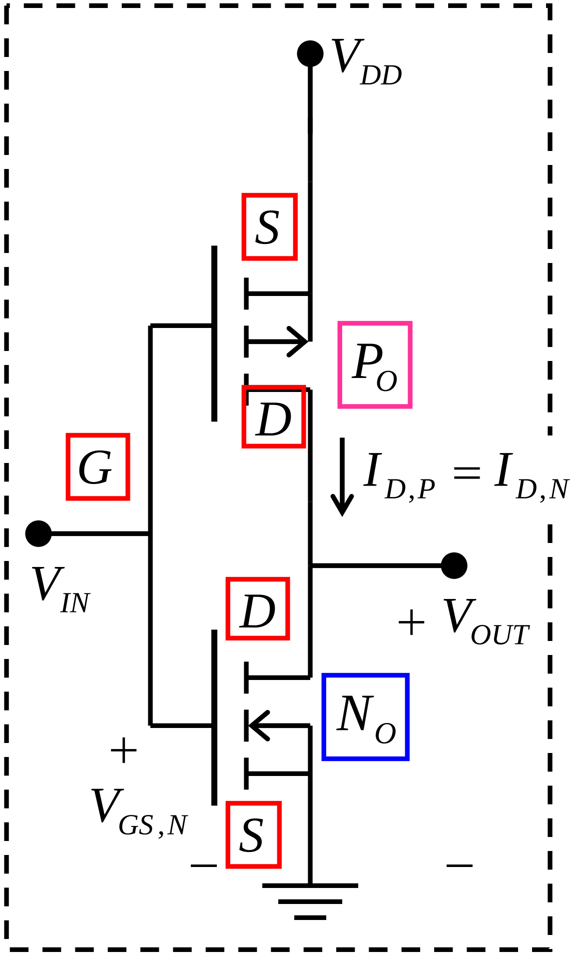
$$\boxed{I_{DS,N}(LIN)=\frac{K_n}{2}\left[2\times(V_{GS,N}-V_{TN})V_{DS,N}-V^2_{DS,N}\right]=0}$$

$$V_{DS,N}\{2\times(V_{GS,N}+V_{TN})-V_{DS,N}\}=0$$

$$V_{DS,N}=0$$

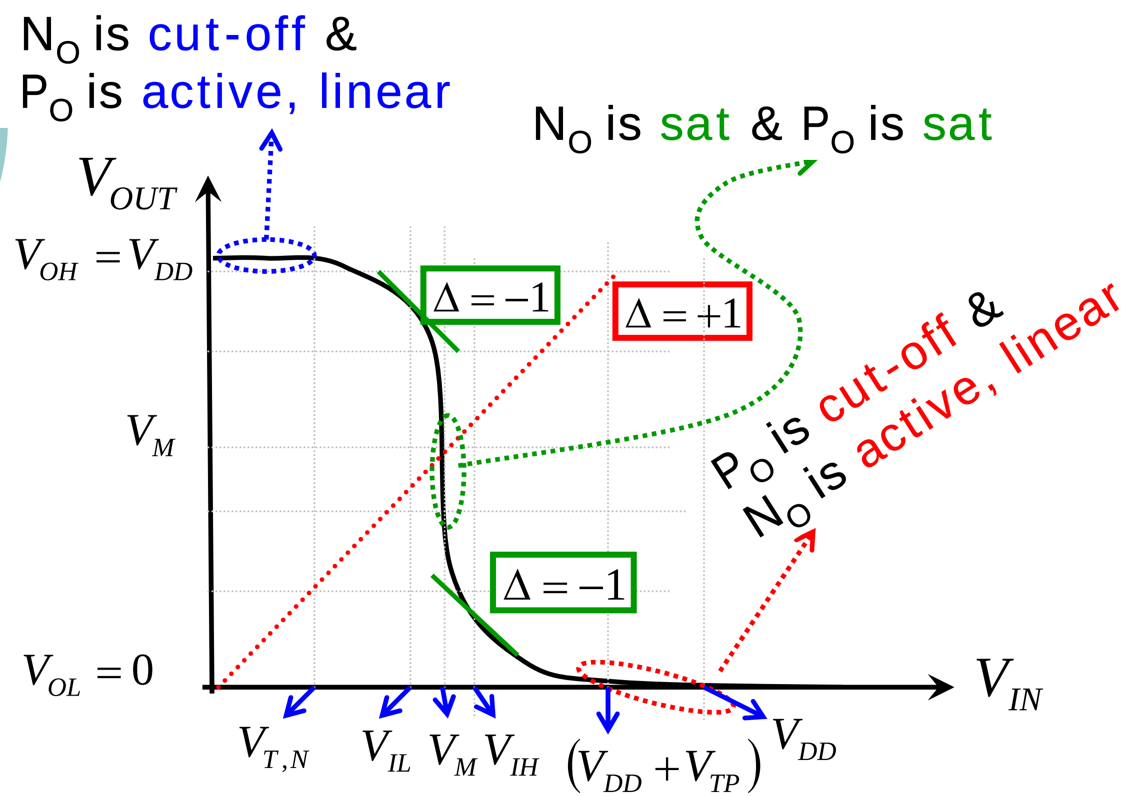
$$V_{DS,N}=2\times(V_{GS,N}-V_{TN})>V_{GS,N}-V_{TN}$$

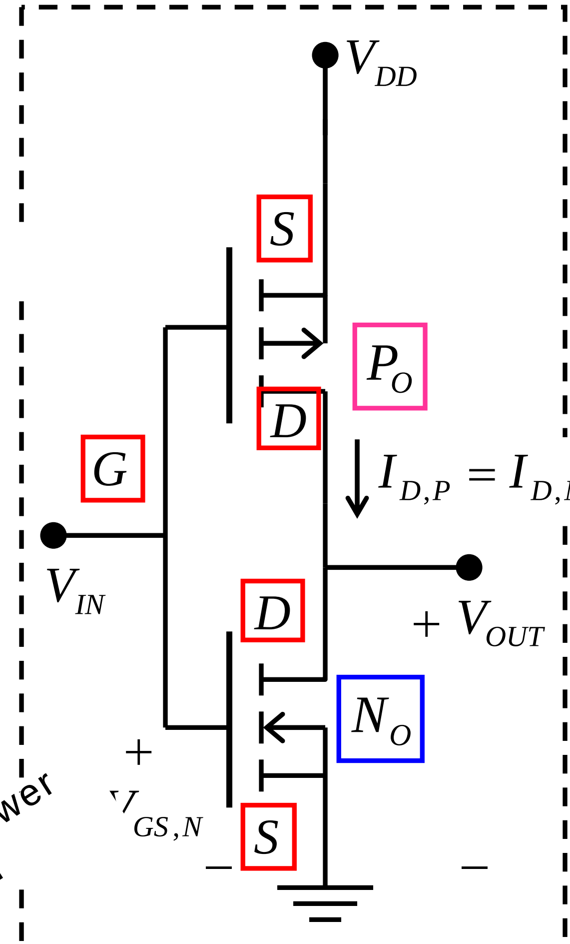
$$\boxed{V_{OL}=V_{DS,N}=0}$$



Invalid since V_{DS} has to be less than $(V_{GS}-V_{TN})$

VTC of CMOS Inverter





for $V_O = V_{OH} (V_I < V_{IL})$ → N_O is cut-off & P_O is linear

for $V_I = V_{IL}$ → N_O is sat & P_O is linear

for $V_I = V_O = V_M$ → N_O is sat & P_O is sat

for $V_I = V_{IH}$ → N_O is linear & P_O is sat

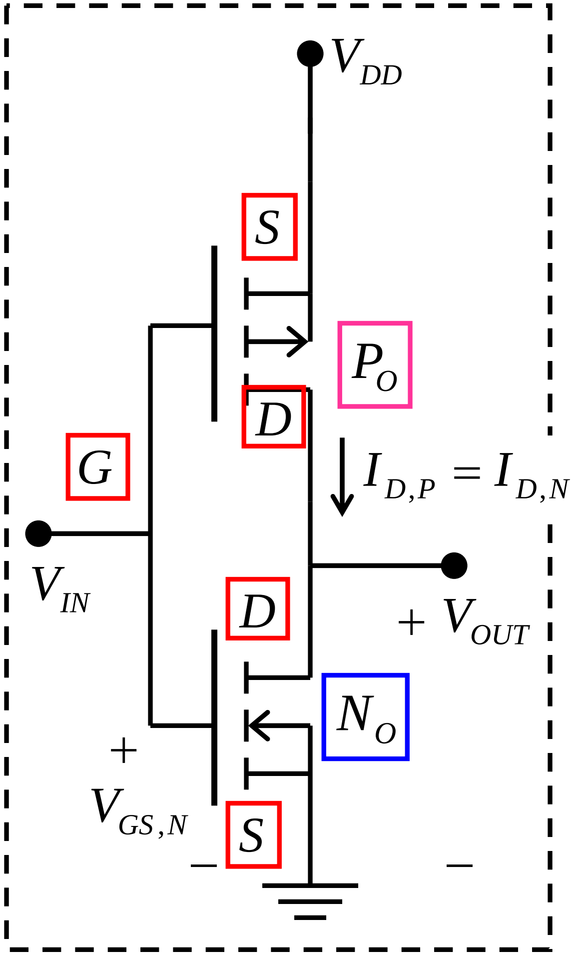
for $V_O = V_{OL}$ → N_O is linear & P_O is cut-off

Dynamic power dissipation

Power Dissipation CMOS Inverter

$I_{DD}(OL)$ ➡ → P_O is cut-off

$I_{DD}(OH)$ ➡ → N_O is cut-off



Static Power Dissipation **$P_{DD}(avg)$**

$$P_{DD}(avg) = V_{DD}\left(\frac{I_{DD}(OL) + I_{DD}(OH)}{2}\right) = 0$$

Power Dissipation CMOS Inverter

Dynamic Power Dissipation $P_{DD}(dyn)$

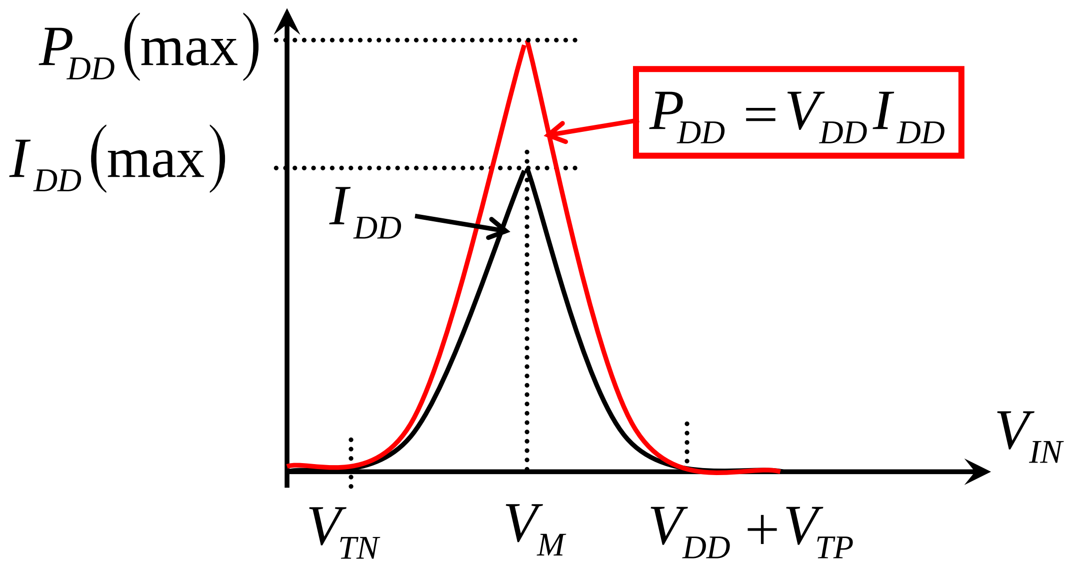
$$\boxed{P_{DD}(dyn) = C_L \upsilon (V_{DD})^2}$$

C_L is the total load capacitance at the output of the gate

υ is the switching frequency of the gate

$$\boxed{P_{DD}(CMOS) = P_{DD}(dyn)}$$

See example 23.1



VTC of CMOS Inverter

Analytical determination of VTC :

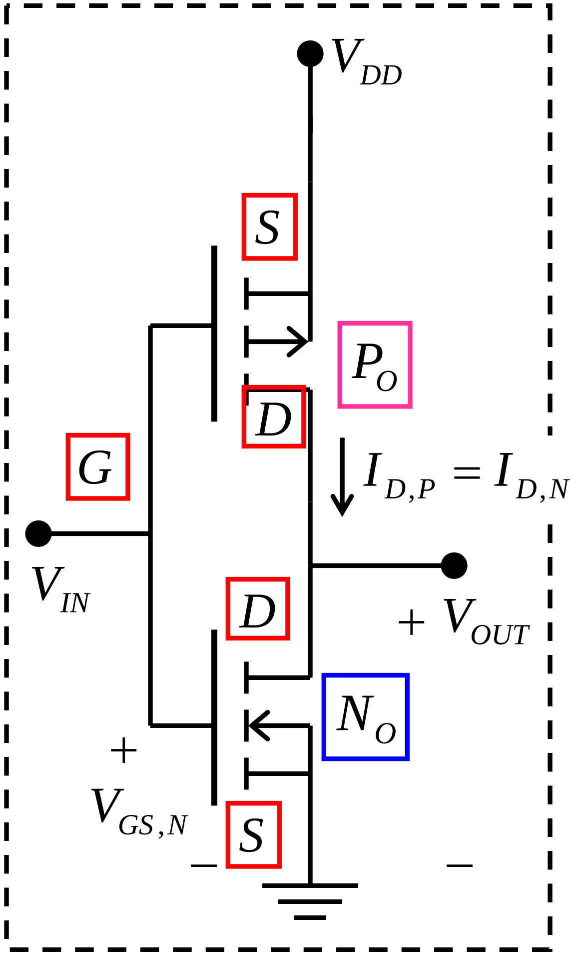
$\boxed{V_{OH}}$

for $V_O = V_{OH} (V_I < V_{IL}) \longrightarrow$

N_O is cut-off & P_O is linear

$$I_{D,N} = I_{D,P} = 0$$

$$\boxed{V_{OH} = V_{DD}} \quad \boxed{V_{DS,N} = V_{DD}}$$



$\boxed{V_{OL}}$

for $V_O = V_{OL} \longrightarrow$ N_O is linear & P_O is cut-off

$$I_{D,N} = I_{D,P} = 0$$

$$\boxed{V_{OL} = 0} \quad \boxed{V_{DS,N} = 0}$$

VTC of CMOS Inverter

Analytical determination of VTC :

$\boxed{V_{IL}}$ for $V_I = V_{IL}$ → N_O is sat & P_O is linear

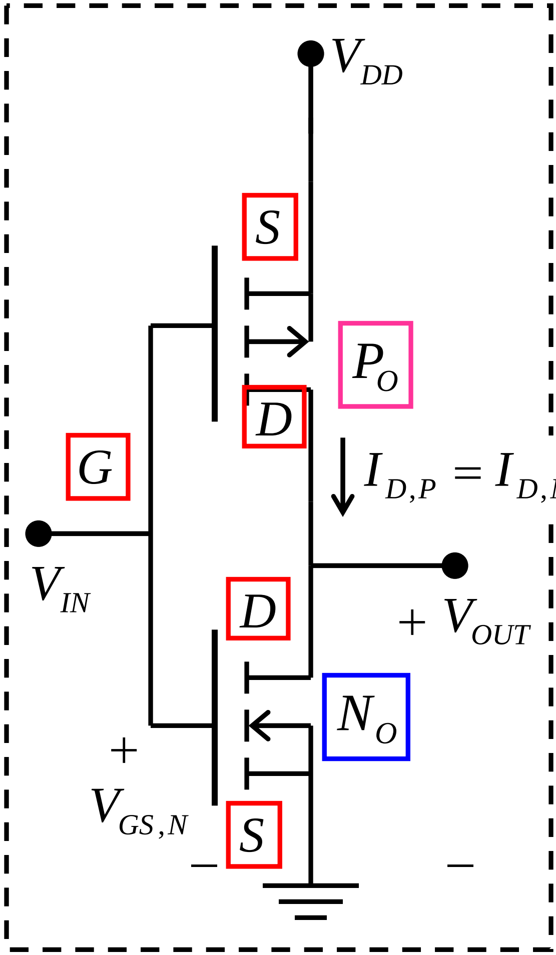
$$\boxed{\begin{array}{ll} V_{GS} = V_{IL} & V_{SG,P} = V_{DD} - V_{IL} \\ V_{DS,N} = V_{Out} & V_{SD,P} = V_{DD} - V_{Out} \end{array}}$$

$$I_{D,N} = \frac{K_n}{2}(V_{GS} - V_{TN})^2 \Rightarrow \boxed{I_{D,N} = \frac{K_n}{2}(V_{IN} - V_{TN})^2}$$

$$I_{D,p} = \frac{K_p}{2}\left[2\times(V_{SG} + V_{TP})V_{SD} - V_{SD}^2\right]$$

$$\boxed{I_{D,p} = \frac{K_p}{2}\left[2\times(V_{DD} - V_{IN} + V_{TP})(V_{DD} - V_{OUT}) - (V_{DD} - V_{OUT})^2\right]}$$

$\boxed{I_{D,N} = I_{D,P}}$ or $\boxed{\frac{\partial I_{D,N}}{\partial V_{IN}} = \frac{\partial I_{D,P}}{\partial V_{IN}}}$



VTC of CMOS Inverter

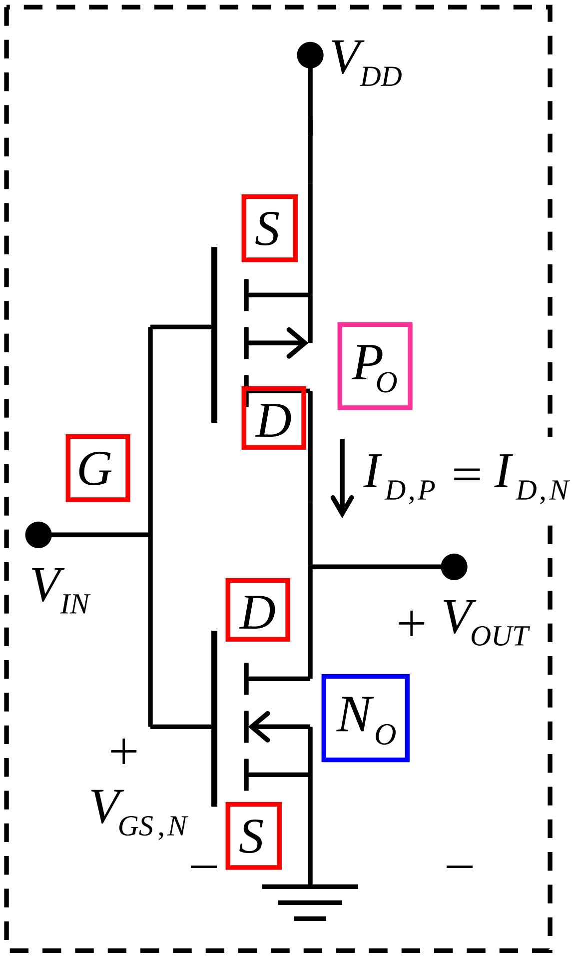
Analytical determination of VTC :

$\boxed{V_{IL}}$ for $V_I = V_{IL}$ $\longrightarrow$ N_O is sat & P_O is linear

$$\boxed{\begin{array}{ll} V_{GS} = V_{IL} & V_{SG,P} = V_{DD} - V_{IL} \\ V_{DS,N} = V_{Out} & V_{SD,P} = V_{DD} - V_{Out} \end{array}}$$

$$\boxed{\left.\frac{dV_{OUT}}{dV_{IN}}\right|_{V_{IN}=V_{IL}} = -1}$$

$$\boxed{V_{IL} = \frac{2K_p V_{OUT} - K_p\left(V_{DD} - V_{TP}\right) + K_n V_{TN}}{K_n + K_p}}$$



VTC of CMOS Inverter

Analytical determination of VTC :

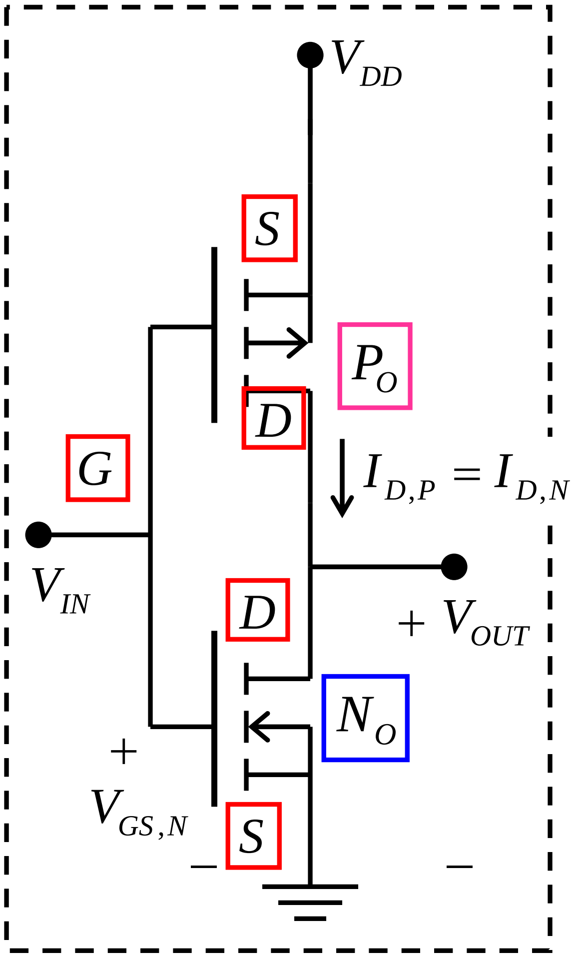
$\boxed{V_{IH}}$ for $V_I = V_{IH}$ → N_O is linear & P_O is sat

$$\begin{array}{ll} V_{GS} = V_{IH} & V_{SG,P} = V_{DD} - V_{IH} \\ V_{DS,N} = V_{Out} & V_{SD,P} = V_{DD} - V_{Out} \end{array}$$

$$I_{D,n} = \frac{K_n}{2}\left[2 \times (V_{IN} - V_{TN})V_{OUT} - V_{OUT}^2\right]$$

$$I_{D,p} = \frac{K_p}{2}(V_{DD} - V_{IN} + V_{TP})^2$$

$$I_{D,N} = I_{D,P} \quad \text{or} \quad \frac{\partial I_{D,N}}{\partial V_{IN}} = \frac{\partial I_{D,P}}{\partial V_{IN}}$$



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VTC of CMOS Inverter

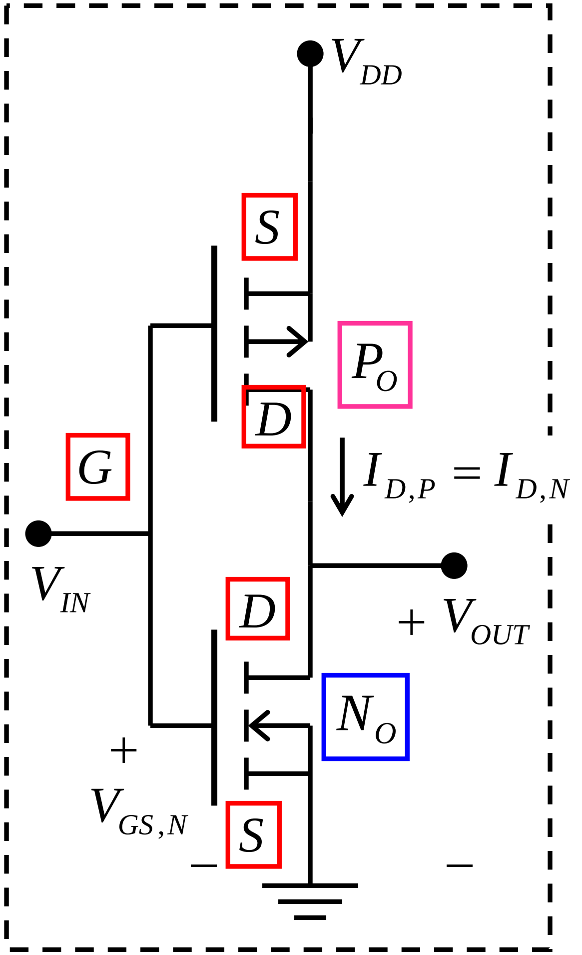
Analytical determination of VTC :

$\boxed{V_{IH}}$ for $V_I = V_{IH}$ → N_O is linear & P_O is sat

$$V_{GS} = V_{IH} \qquad V_{SG,P} = V_{DD} - V_{IH}$$
$$V_{DS,N} = V_{Out} \qquad V_{SD,P} = V_{DD} - V_{Out}$$

$$\left.\frac{dV_{OUT}}{dV_{IN}}\right|_{V_{IN}=V_{IH}} = -1$$

$$V_{IH} = \frac{2K_nV_{OUT} + K_p\left(V_{DD} + V_{TP}\right) + K_nV_{TN}}{K_n + K_p}$$



VTC of CMOS Inverter

Analytical determination of VTC :

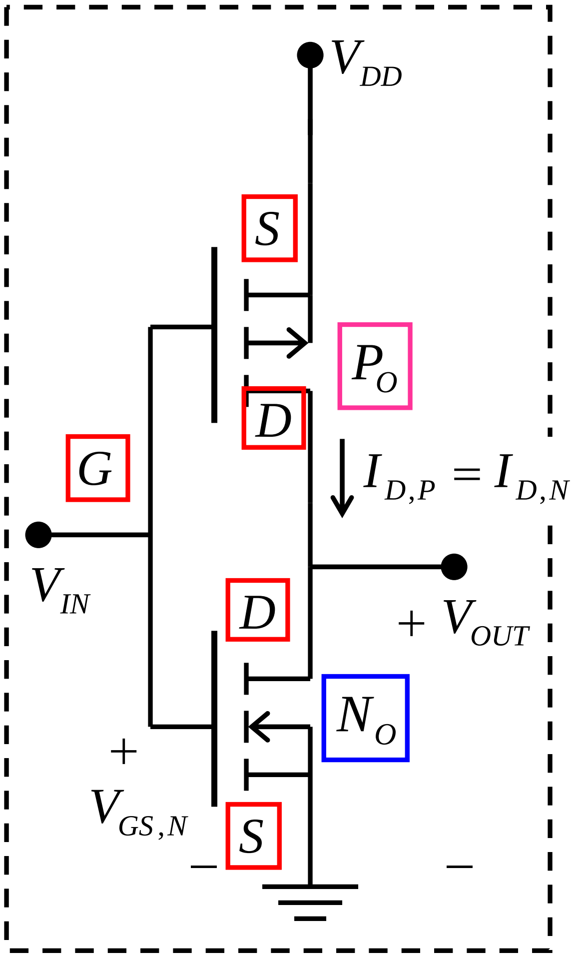
$\boxed{V_M}$ Mid point

for $V_I = V_O = V_M$ → N_O is sat & P_O is sat

$$\boxed{\frac{K_n}{2}\left(V_M - V_{TN}\right)^2 = \frac{K_p}{2}\left(\left(V_{DD} - V_M\right) + V_{TP}\right)^2}$$

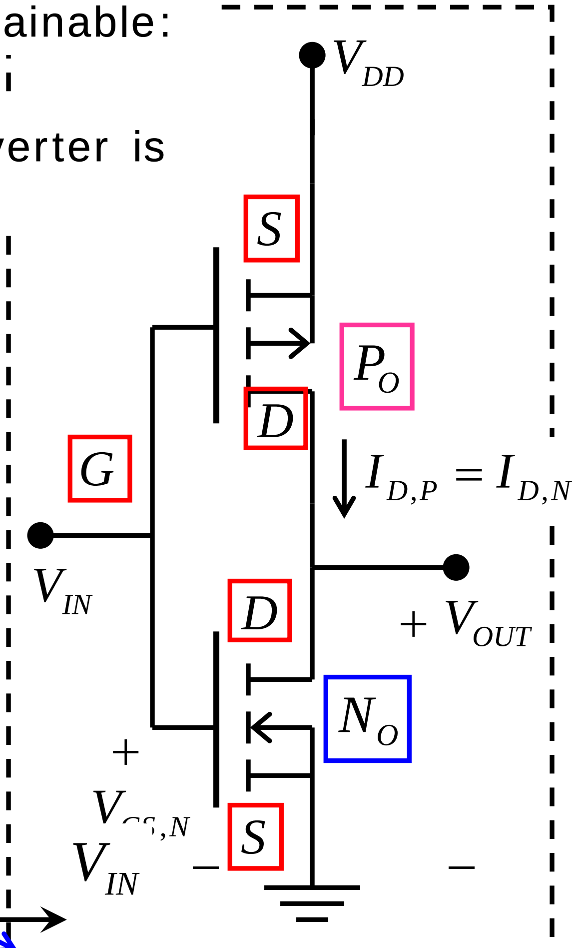
Then solve for V_M

See example on page 342



The Symmetric CMOS Inverter

- The VTC of symmetric CMOS inverter is easily obtainable:
- One reason of designing a symmetric CMOS inverter is to obtain a symmetric transient response:

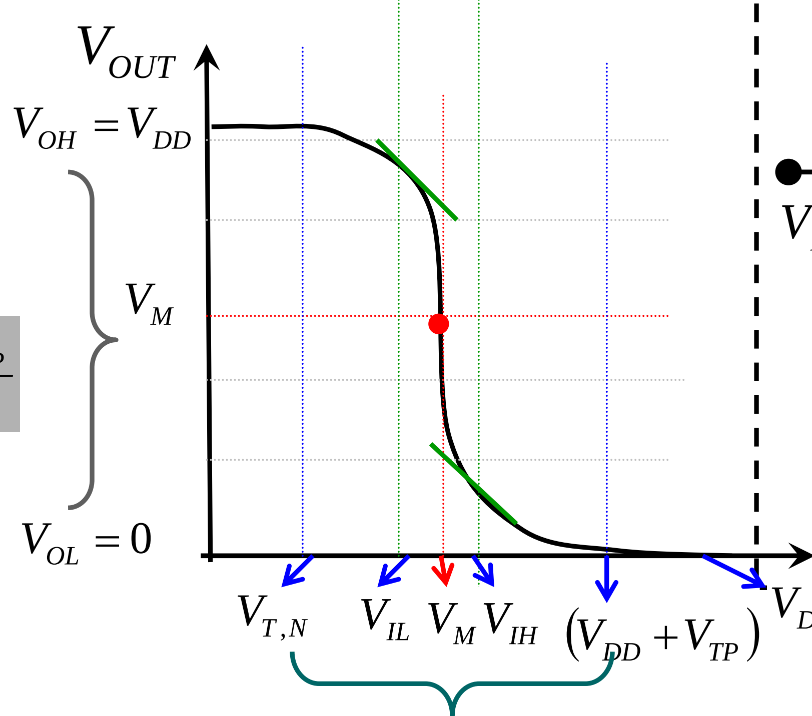


- *Remember the VTC of CMOS inverter*

$$V_M = \frac{V_{OH} + V_{OL}}{2} = \frac{V_{DD}}{2}$$

$$V_M = \frac{V_{IH} + V_{IL}}{2} = \frac{V_{TN} + V_{DD} + V_{TP}}{2}$$

$$V_{TN} = -V_{TP}$$



Design of Symmetric CMOS Inverter

1. The threshold voltages of N-MOS and P-MOS are made equal in magnitude

2. The requirements for $K_n = K_p$ must be considered

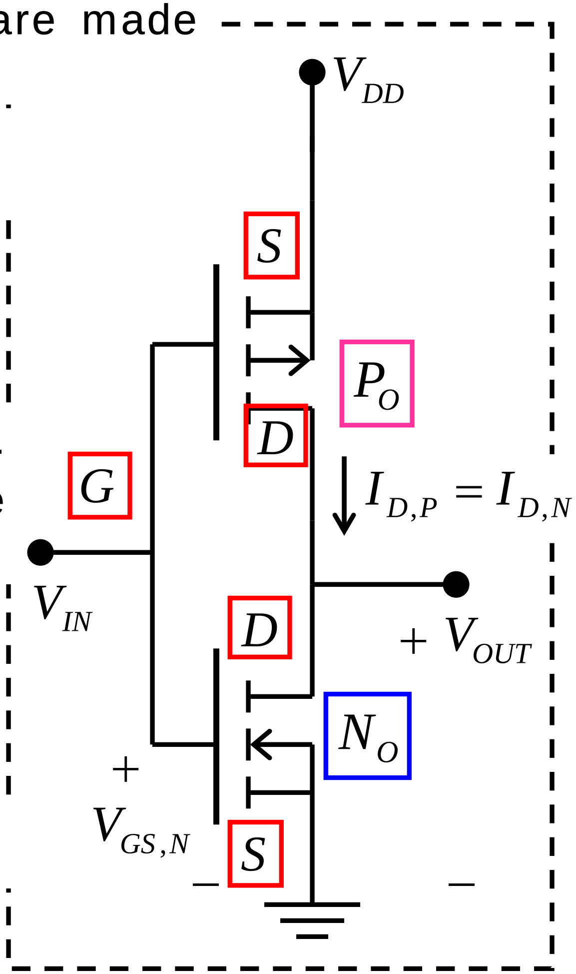
$$K_n = \frac{W_n}{L_n}\mu_n C_{ox} \qquad K_p = \frac{W_p}{L_p}\mu_p C_{ox}$$

3. Usually the gate oxide layers of the N-MOS and P-MOS devices are grown simultaneously, and hence have the <u>same</u> thickness t_{ox}

$$\boxed{\frac{W_n}{L_n}\mu_n = \frac{W_p}{L_p}\mu_p}$$

4. Typically $\mu_n(\mathrm{Si}) = 580\ \mathrm{cm^2/V.s}$ and $\mu_p(\mathrm{Si}) = 230\ \mathrm{cm^2/V.s}$

$$\boxed{\frac{W_p}{L_p} = 2.5\frac{W_n}{L_n}}$$



Design of Symmetric CMOS Inverter

○ Example

Design a symmetrical CMOS inverter assuming:

V_{DD}=5V, V_{TN}=1 V, V_{TP}=-1 V, $\mu_n C_{ox}$=40 µA/V^2 , $\mu_p C_{ox}$=16 µA/V2 , W_n=4 µm, L_n=L_p=2 µm

And verify that the midpoint voltage is half of V_{DD}, and V_{IL} and V_{IH} are symmetric about V_M.

○ Solution

For symmetry, the width of the channel of P-MOS is determined from

$$\boxed{\frac{W_p}{L_p} = 2.5\frac{W_n}{L_n}} \Rightarrow \boxed{W_p = 2.5\times 4 = 10\mu m}$$

$$K_n = \frac{W_n}{L_n}\mu_n C_{ox} \qquad K_n = 2\times 40 = 80\mu A/V^2$$

Equal values

$$K_p = \frac{W_p}{L_p}\mu_p C_{ox} \qquad K_p = 5\times 16 = 80\mu A/V^2$$

Design of Symmetric CMOS Inverter

- Example

Design a symmetrical CMOS inverter assuming:

V_{DD}=5V, V_{TN}=1 V, V_{TP}=-1 V, $\mu_n C_{ox}$=40 µA/V^2 , $\mu_p C_{ox}$=16 µA/V2 , W_n=4 µm, L_n=L_p=2 µm

And verify that the midpoint voltage is half of V_{DD}, and V_{IL} and V_{IH} are symmetric about V_M.

- Solution

$$\boxed{\frac{K_n}{2}(V_M - V_{TN})^2 = \frac{K_p}{2}((V_{DD} - V_M) + V_{TP})^2}$$

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$$\boxed{(V_M - 1)^2 = ((5 - V_M) - 1)^2}$$

$$\boxed{2V_M = 5 \Rightarrow V_M = 2.5V} \Rightarrow \boxed{V_M = \frac{V_{DD}}{2}}$$

Design of Symmetric CMOS Inverter

- Example

Design a symmetrical CMOS inverter assuming:

V_{DD}=5V, V_{TN}=1 V, V_{TP}=-1 V, $\mu_n C_{ox}$=40 µA/V^2 , $\mu_p C_{ox}$=16 µA/V2 , W_n=4 µm, L_n=L_p=2 µm

And verify that the midpoint voltage is half of V_{DD}, and V_{IL} and V_{IH} are symmetric about V_M.

- Solution

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$$\boxed{V_{IL} = \frac{2K_pV_{OUT} - K_p(V_{DD} - V_{TP}) + K_nV_{TN}}{K_n + K_p}} \Rightarrow \boxed{V_{IL} = \frac{160V_{OUT} - 80(5+1) + 80}{160} = V_{OUT} - 2.5}$$

$$I_{D,N} = \frac{K_n}{2}(V_{IN} - V_{TN})^2 = I_{D,p} = \frac{K_p}{2}\left[2\times(V_{SG} + V_{TP})V_{SD} - V_{SD}^2\right]$$

$$\frac{K_n}{2}(V_{IL} - V_{TN})^2 = \frac{K_p}{2}\left[2\times((V_{DD} - V_{IL}) + V_{TP})(V_{DD} - V_{OUT}) - (V_{DD} - V_{OUT})^2\right]$$

$$(V_{IL} - 1)^2 = \left[2\times((5 - V_{IL}) - 1)(5 - V_{IL} - 2.5) - (5 - V_{IL} - 2.5)^2\right]$$

Design of Symmetric CMOS Inverter

- Example

Design a symmetrical CMOS inverter assuming:

$V_{DD}=5V$, $V_{TN}=1$ V, $V_{TP}=-1$ V, $\mu_n C_{ox}=40\ \mu A/V^2$, $\mu_p C_{ox}=16\ \mu A/V2$, $W_n=4\ \mu m$, $L_n=L_p=2\ \mu m$

And verify that the midpoint voltage is half of V_{DD}, and V_{IL} and V_{IH} are symmetric about V_M.

- Solution

$$(V_{IL}-1)^2=\left[2\times((5-V_{IL})-1)(5-V_{IL}-2.5)-(5-V_{IL}-2.5)^2\right]$$

$$(V_{IL}-1)^2=\left[2\times(4-V_{IL})(2.5-V_{IL})-(2.5-V_{IL})^2\right] \Rightarrow \boxed{V_{IL}=\frac{12.75}{6}=2.125V}$$

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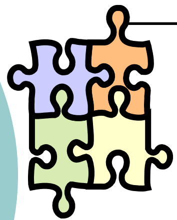
Design of Symmetric CMOS Inverter



- Example

Design a symmetrical CMOS inverter assuming:

V_{DD}=5V, V_{TN}=1 V, V_{TP}=-1 V, $\mu_n C_{ox}$=40 µA/V^2 , $\mu_p C_{ox}$=16 µA/V2 ,
W_n=4 µm, L_n=L_p=2 µm

And verify that the midpoint voltage is half of V_{DD}, and V_{IL} and V_{IH} are symmetric about V_M.

- Solution :similarly

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$$\boxed{V_{IH} = \frac{2K_n V_{OUT} + K_p\left(V_{DD} + V_{TP}\right) + K_n V_{TN}}{K_n + K_p}} \Rightarrow \boxed{V_{IH} = \frac{160V_{OUT} + 80(5-1) + 80}{160} = V_{OUT} + 2.5}$$

$$I_{D,N} = \frac{K_n}{2}\left(V_{IN} - V_{TN}\right)^2 = I_{D,p} = \frac{K_p}{2}\left[2\times\left(V_{SG} + V_{TP}\right)V_{SD} - V_{SD}^2\right]$$

$$\frac{K_n}{2}\left(V_{IH} - V_{TN}\right)^2 = \frac{K_p}{2}\left[2\times\left(\left(V_{DD} - V_{IH}\right) + V_{TP}\right)\left(V_{DD} - V_{OUT}\right) - \left(V_{DD} - V_{OUT}\right)^2\right]$$

$$\left(V_{IH} - 1\right)^2 = \left[2\times\left(\left(5 - V_{IH}\right) - 1\right)\left(5 - V_{IH} + 2.5\right) - \left(5 - V_{IH} + 2.5\right)^2\right] \Rightarrow \boxed{V_{IH} = 2.875V}$$

Design of Symmetric CMOS Inverter

- Example

Design a symmetrical CMOS inverter assuming:

V_{DD}=5V, V_{TN}=1 V, V_{TP}=-1 V, $\mu_n C_{ox}$=40 μA/V^2 , $\mu_p C_{ox}$=16 μA/V2 , W_n=4 μm, L_n=L_p=2 μm

And verify that the midpoint voltage is half of V_{DD}, and V_{IL} and V_{IH} are symmetric about V_M.

- Solution

$$V_{IL} = 2.125V$$

$$V_{IH} = 2.875V$$

$$\frac{V_{IH} + V_{IL}}{2} = \frac{2.875 + 2.125}{2} = 2.5V = V_M$$

V_{IL} and V_{IH} are symmetric about V_M.

- HW #12:Solve Problems: 23.**1-3**, 23.22